KILPATRICK TOWNSEND

Barmak S. Sani

Partner

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Services

Asset Creation - Prosecution & Counseling

Intellectual Property

Post-Grant Proceedings

Industries

Technology

Barmak Sani focuses his practice on patent counseling. Mr. Sani has assisted domestic and international companies including numerous Silicon Valley start-ups in building and managing patent portfolios as well as analyzing patents in a variety of contexts including infringement/validity opinions, reexamination and reissue proceedings, design around efforts, and litigation. He has also provided in-depth analysis of patent portfolios in the context of licensing negotiations, venture capital investments, and corporate acquisitions.

Mr. Sani has extensive experience in the prosecution of foreign and domestic patents in a variety of electronics fields, including volatile and non-volatile semiconductor memories, solid state drive (SSD) systems, semiconductor power devices, semiconductor process and packaging, electronic design automation (EDA), and ICs for wireless, home networking, and mobile TV applications.

Prior to joining the legal profession, Mr. Sani worked at Signetics Corporation as a circuit designer, and later at a start-up company, Wafer Scale Integration, Inc., managing a team of integrated circuit designers primarily responsible for the design and development of high performance non-volatile memory products. He has nine years of industry experience in the area of non-volatile memory technology. Mr. Sani holds two patents and has published and presented a number of articles related to non-volatile memories.

Mr. Sani served as a co-leader of Kilpatrick Townsend's Electronics & Software Practice Group for four years and prior to that served as the hiring partner for the Electronics & Software Practice Group for three years. Mr. Sani currently serves on the advisory board for Santa Clara University School of Law, High Tech Law Institute.

Experience

Representing a successful packaging company in an *Inter Partes* reexamination of a patent relating to semiconductor packaging technology. The patent is asserted against our client in concurrent litigation.

Representing a successful semiconductor startup company in *Inter Partes* reexaminations of 4 patents relating

to non-volatile memory technology. Three of the four patents are asserted against our client in concurrent litigation, and the fourth *Inter Partes* reexamination was initiated on one of our client's patents by the opposing party.

Drafted *ex parte* reexam requests on seven patents for two semiconductor companies.

Education

Santa Clara University School of Law, J.D. (1997)

Santa Clara University School of Engineering, M.S., Electrical Engineering (1991)

University of California, Berkeley, B.S., Electrical Engineering (1983)

Admissions

California (1998)

Court Admissions

U.S. District Court for the Northern District of California (2010)

U.S. Patent and Trademark Office (1998)

Professional & Community Activities

Santa Clara University School of Law, High Tech Advisory Board Member

American Bar Association

American Intellectual Property Law Association, Member

Iranian American Bar Association, Member

Insights

In The News

Kilpatrick Townsend's Media Report March 6-12, 2015

March 13, 2015